What is claimed is:

[c1] 1.A method for separating exception vectors in a data processing system having at least two processors, comprising the steps of:
receiving an exception request into one of the at least two processors;
entering, in the processor receiving the exception request, an exception mode relating to the received exception request;
calling an instruction located at a portion of an exception vector table associated with the type of exception request received, wherein the instruction causes the moving of a register into a program counter register of the processor receiving the exception request; and
executing a processor-specific exception handling routine relating to the received exception request, the address of the processor-specific exception handling routine being maintained in the register.

[c2] 2.The method of claim 1, wherein the step of entering an exception mode, further comprises the step of replacing a normal register in the processor receiving the exception request with a processor-specific exception mode banked register.

[c3] 3.The method of claim 2, wherein the register moved into the program counter is the processor-specific exception mode banked register.

[c4] 4.The method of claim 1, further comprising the step of initializing the processor-specific exception mode banked register to contain the address of the exception handling routine.

[c5] 5.The method of claim 1, wherein the exception request is an interrupt request (IRQ).

[c6] 6.The method of claim 5, wherein the processor-specific exception mode banked register is a processor-specific IRQ mode banked register.

[c7] 7.The method of claim 1, wherein the instruction located at a portion of an exception vector table associated with the type of exception request received, is an instruction taking the form "move pc, r13", indicating that the contents of the r13 register are to be moved into the program counter register.

[c8] 8.The method of claim 1, wherein the at least two processor are reduced instruction set computing (RISC) processors.

[c9] 9.A data processing system for separating exception vectors, comprising:
at least two processors for executing a plurality of instructions;
a memory shared by the at least two processors, the memory containing at least an exception vector table common to the at least two processors;
means for receiving an exception request into one of the at least two processors;
means for entering, in the processor receiving the exception request, an exception mode relating to the received exception request;
means for calling an instruction located at a portion of the exception vector table associated with the type of exception request received, wherein the instruction causes the moving of a register into a program counter register of the processor receiving the exception request; and
means for executing a processor-specific exception handling routine relating to the received exception request, the address of the processor-specific exception handling routine being maintained in the register.

[c10] 10.The data processing system of claim 9, wherein the means for entering an exception mode, further comprise means for replacing a normal register in the processor receiving the exception request with a processor-specific exception mode banked register.

[c11] 11.The data processing system of claim 10, wherein the register moved into the program counter is the processor-specific exception mode banked register.

[c12] 12.The data processing system of claim 9, further comprising means for initializing the processor-specific exception mode banked register to contain the address of the exception handling routine.

[c13] 13.The data processing system of claim 9, wherein the exception request is an interrupt request (IRQ).

[c14] 14.The data processing system of claim 13, wherein the processor-specific exception mode banked register is a processor-specific IRQ mode banked

register.

[c15] 15.The data processing system of claim 9, wherein the instruction located at a portion of an exception vector table associated with the type of exception request received, is an instruction taking the form "move pc, r13", indicating that the contents of the r13 register are to be moved into the program counter register.

[c16] 16.The data processing system of claim 9, wherein the at least two processor are reduced instruction set computing (RISC) processors.

[c17] 17. A computer readable medium incorporating one or more instructions for separating exception vectors in a data processing system having at least two processors, the instructions comprising:
one or more instructions for receiving an exception request into one of the at least two processors;
one or more instructions for entering, in the processor receiving the exception request, an exception mode relating to the received exception request;
one or more instructions for calling an instruction located at a portion of an exception vector table associated with the type of exception request received, wherein the instruction causes the moving of a register into a program counter register of the processor receiving the exception request; and
one or more instructions for executing a processor-specific exception handling routine relating to the received exception request, the address of the processor-specific exception handling routine being maintained in the register.

[c18] 18.The computer readable medium of claim 17, wherein the one or more instructions for entering an exception mode, further comprises one or more instructions for replacing a normal register in the processor receiving the exception request with a processor-specific exception mode banked register.

[c19] 19.The computer readable medium of claim 18, wherein the register moved into the program counter is the processor-specific exception mode banked register.

[c20] 20.The computer readable medium of claim 17, the instructions further comprising one or more instructions for initializing the processor-specific

exception mode banked register to contain the address of the exception handling routine.

[c21] 21.The computer readable medium of claim 17, wherein the exception request is an interrupt request (IRQ).

[c22] 22.The computer readable medium of claim 21, wherein the processor-specific exception mode banked register is a processor-specific IRQ mode banked register.

[c23] 23.The computer readable medium of claim 17, wherein the instruction located at a portion of an exception vector table associated with the type of exception request received, is an instruction taking the form "move pc, r13", indicating that the contents of the r13 register are to be moved into the program counter register.

[c24] 24.The computer readable medium of claim 17, wherein the at least two processor are reduced instruction set computing (RISC) processors.